SYNCHRONIZATION POINT ACROSS DIFFERENT MEMORY BIST CONTROLLERS

ABSTRACT OF THE DISCLOSURE

A circuit is disclosed for testing memories using multiple built-in self test (BIST) controllers embedded in an integrated circuit (IC). The BIST controllers are brought to a synchronization point during the memory test by allowing for a synchronization state. An output signal from an output pin on the IC indicates the existence of a synchronization state to automated test equipment (ATE). After an ATE receives the output signal, it issues a resume signal through an IC input pin that causes the controllers to advance out of the synchronization state. The ATE controls the synchronization state length by delaying the resume signal. Synchronization states can be used in parametric test algorithms, such as for retention and IDDQ tests. Synchronization states can be incorporated into user-defined algorithms by software design tools that generate an HDL description of a BIST controller operable to apply the algorithm with the synchronization state.